Datasheet October 30, 2008 FN9218.2

High Current LDO with Low I_Q and High PSRR

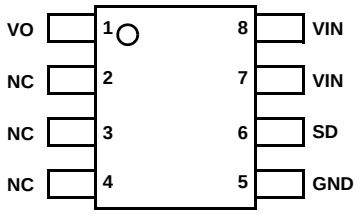
ISL9007 is a high performance LDO that delivers a continuous 400mA of load current. It has a low standby current and high PSRR and is stable with output capacitance of 1µF to 10µF with an ESR of up to 200mΩ.

The ISL9007 has a very high PSRR of 75dB and output noise less than 30µV_{RMS}. When coupled with a no load quiescent current of 50µA (typical), and 1µA (max) shutdown current, the ISL9007 is an ideal choice for portable wireless equipment.

The ISL9007 comes in fixed voltage options of 3.3V, 2.85V, 2.8V, and 2.5V with ±1.8% output voltage accuracy over-temperature, line and load. Other output voltage options may be available upon request.

Pinout

ISL9007
(8 Ld MSOP)
TOP VIEW



Features

- High performance LDO with 400mA continuous output
- Excellent transient response to large current steps
- Excellent load regulation: <0.1% voltage change across full range of load current
- Very high PSRR: 75dB @ 1kHz
- Wide input voltage capability: 2.3V to 6.5V
- Very low quiescent current: 50µA
- Low dropout voltage: typically 200mV @ 400mA
- Low output noise: typically 30µV_{RMS} @ 100µA (2.5V)
- Stable with 1µF to 10µF ceramic capacitors
- Shutdown pin turns off LDO for 1µA (max) standby current
- Soft-start to limit input current surge during enable
- Current limit and overheat protection
- ±1.8% accuracy over all operating conditions
- 8 Ld MSOP package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices, including Medical Handhelds

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	VO VOLTAGE (V) (Note 3)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9007IUNZ*	007NZ	3.3	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUKZ*	007KZ	2.85	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUJZ*	007JZ	2.8	-40 to +85	8 Ld MSOP	M8.118
ISL9007IUFZ*	007FZ	2.5	-40 to +85	8 Ld MSOP	M8.118

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. For other output voltages, contact Intersil Marketing.

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . +7.1V
VO Pin . . . . . +3.6V
All Other Pins . . . . . -0.3 to (VIN + 0.3)V

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +85°C
Supply Voltage (VIN) . . . . . 2.3V to 6.5V

Thermal Information

Thermal Resistance (Typical, Notes 4, 5) θ_{JA} (°C/W)
8 Ld MSOP Package 157
Junction Temperature . . . . . -40°C to +125°C
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:
T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		2.3		6.5	V
Ground Current	I_{DD}	Quiescent condition: I_O = 0µA		50	70	µA
Shutdown Current	I_{DDS}	@ +25°C		0.1	1.0	µA
UVLO Threshold	V_{UV+}		1.9	2.1	2.3	V
	V_{UV-}		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Initial accuracy at V_{IN} = V_O + 0.5V, I_O = 10mA, T_J = +25°C	-0.7		+0.7	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 400mA, T_J = +25°C	-0.8		+0.8	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 400mA, T_J = -40°C to +125°C	-1.8		+1.8	%
Maximum Output Current	I_{MAX}	Continuous	400			mA
Internal Current Limit	I_{LIM}		470	540	750	mA
Drop-out Voltage (Note 7)	V_{DO1}	I_O = 400mA; 2.5V ≤ V_O ≤ 2.8V		250	400	mV
	V_{DO2}	I_O = 400mA; 2.8V < V_O		200	325	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 6)		I_O = 10mA, V_{IN} = 2.8V (min), V_O = 1.8V				
		@ 1kHz		75		dB
		@ 10kHz		60		dB
		@ 100kHz		40		dB
Output Noise Voltage (Note 6)		I_O = 100µA, V_O = 1.5V, T_A = +25°C BW = 10Hz to 100kHz		40		μV_{RMS}
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO (nom)		250	500	µs
LDO Soft-start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	µs/V

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:
T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SD PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.4	V
Input High Voltage	V_{IH}		1.4		V_{IN} + 0.3	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	µA
Pin Capacitance	C_{PIN}	Informative		5		pF

NOTES:

6. Limits established by characterization and are not production tested.
7. VO-x = 0.98*VO-x(NOM).
8. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

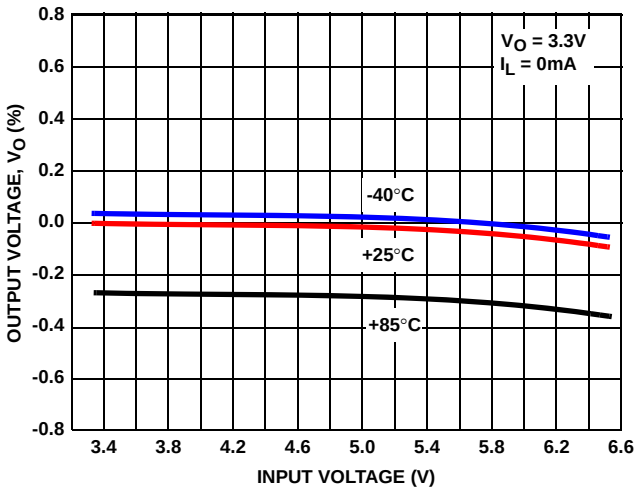


FIGURE 1. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

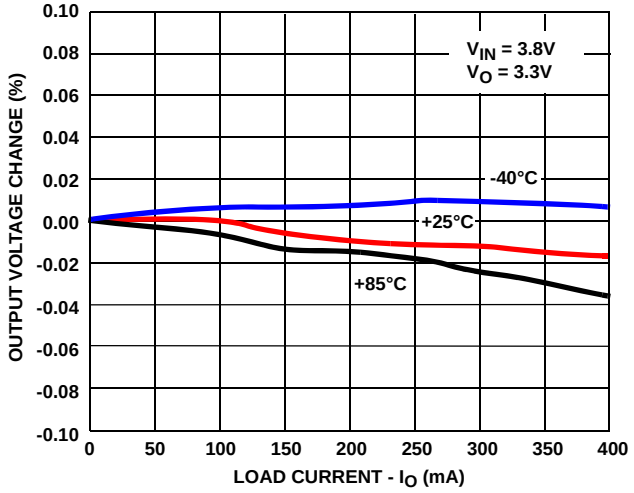


FIGURE 2. OUTPUT VOLTAGE vs LOAD CURRENT

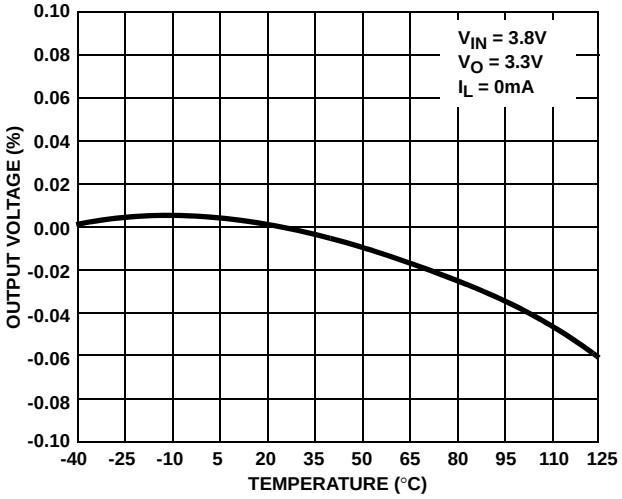


FIGURE 3. OUTPUT VOLTAGE vs TEMPERATURE

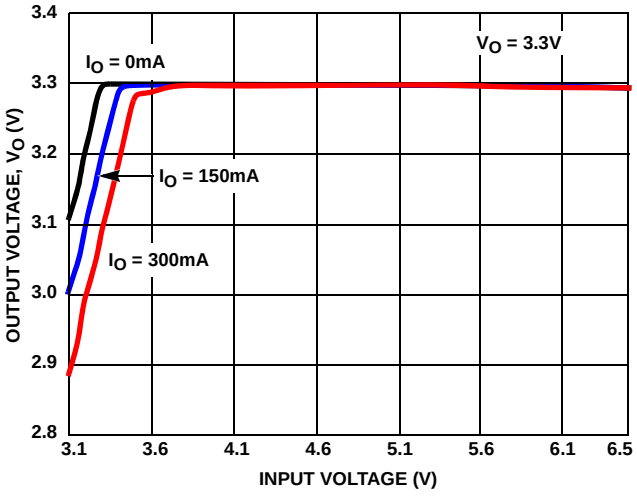


FIGURE 4. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

Typical Performance Curves

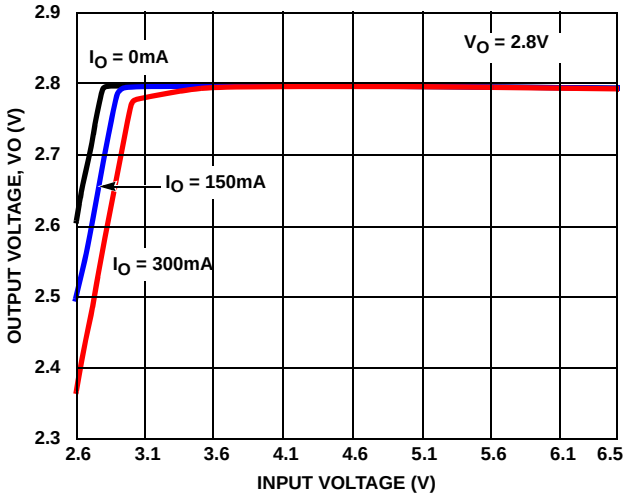


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

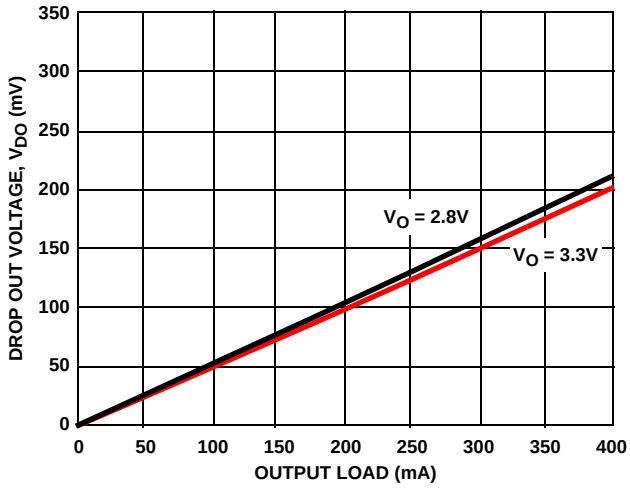


FIGURE 6. DROPOUT VOLTAGE vs LOAD CURRENT

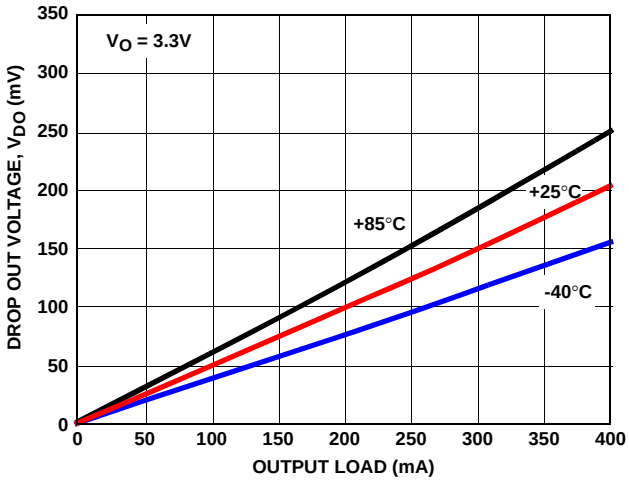


FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

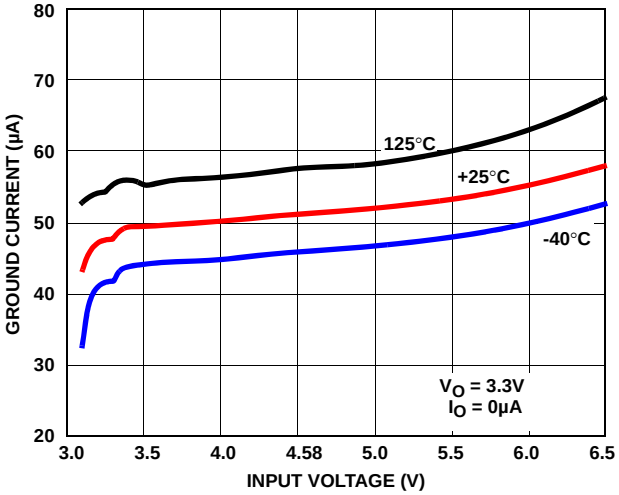


FIGURE 8. GROUND CURRENT vs INPUT VOLTAGE

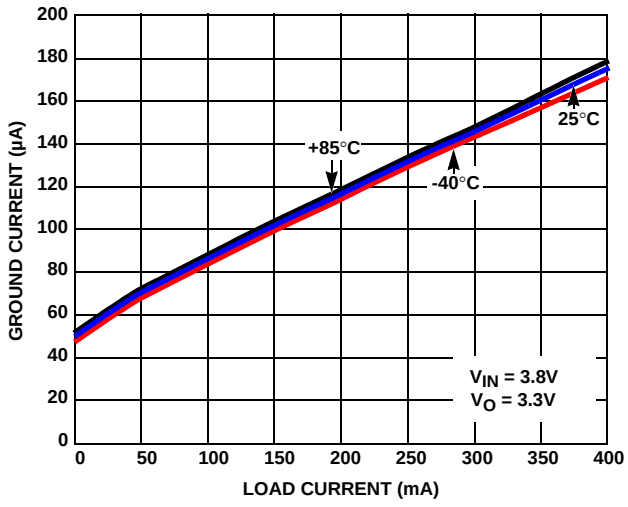


FIGURE 9. GROUND CURRENT vs LOAD

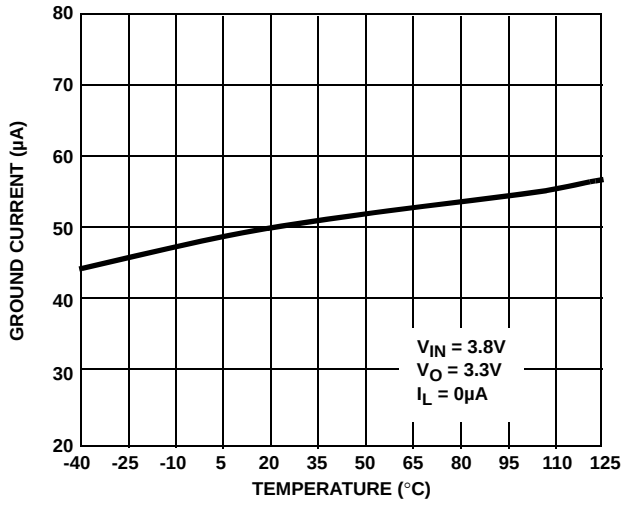


FIGURE 10. GROUND CURRENT vs TEMPERATURE

Typical Performance Curves

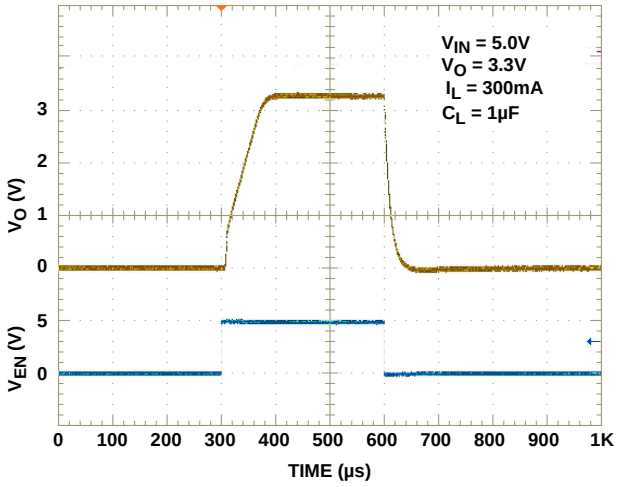


FIGURE 11. TURN ON/TURN OFF RESPONSE

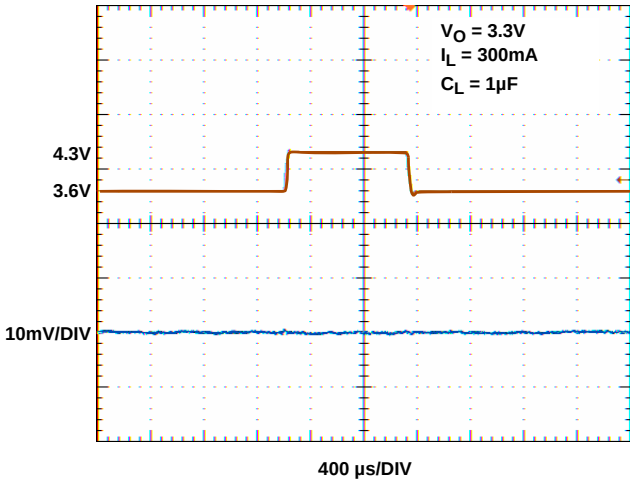


FIGURE 12. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

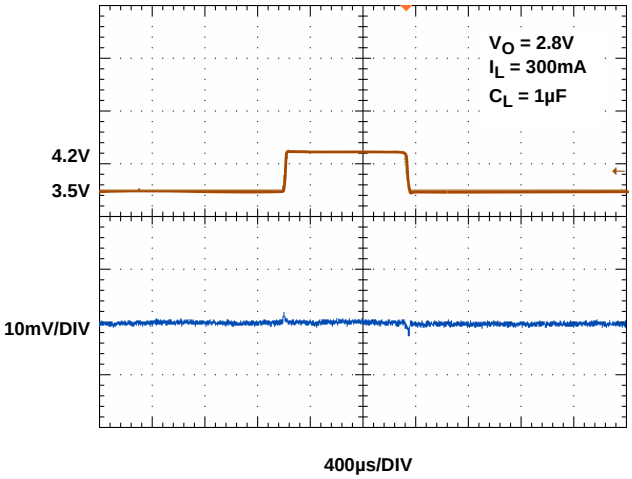


FIGURE 13. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

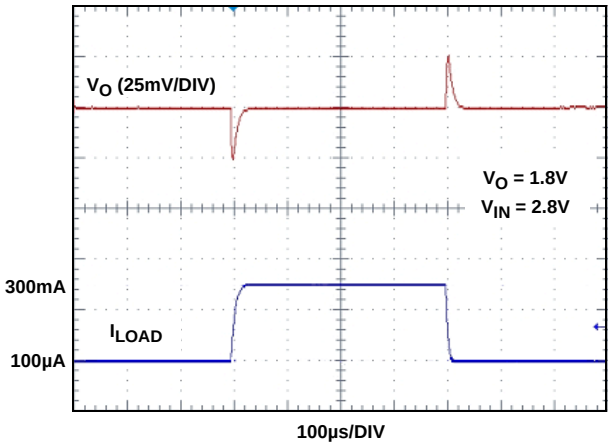


FIGURE 14. LOAD TRANSIENT RESPONSE

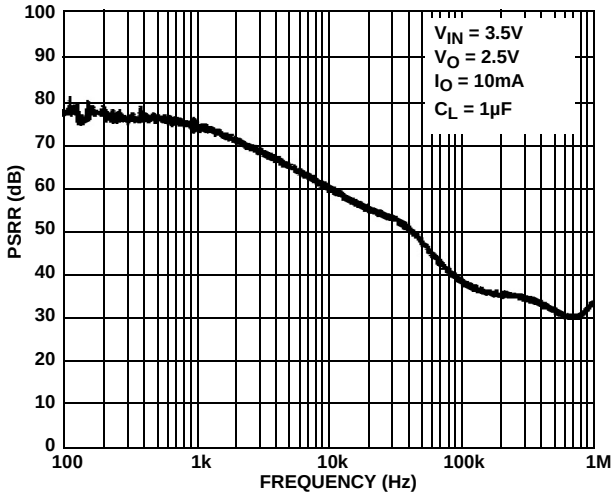


FIGURE 15. PSRR vs FREQUENCY

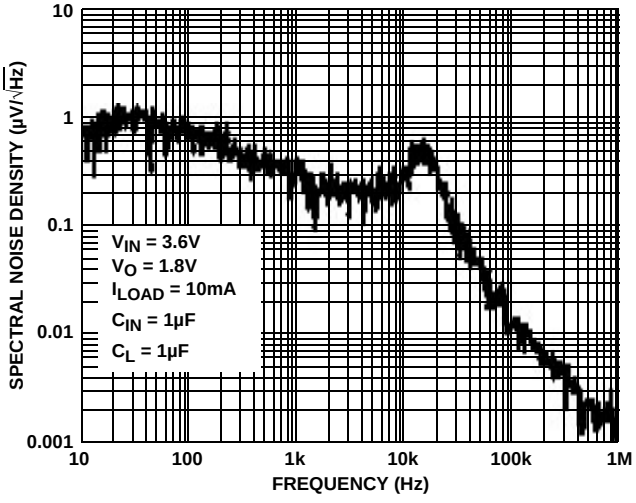
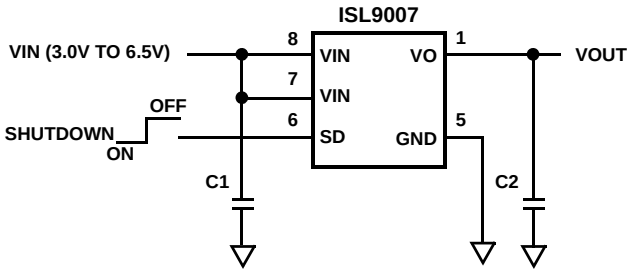


FIGURE 16. SPECTRAL NOISE DENSITY vs FREQUENCY

Pin Descriptions

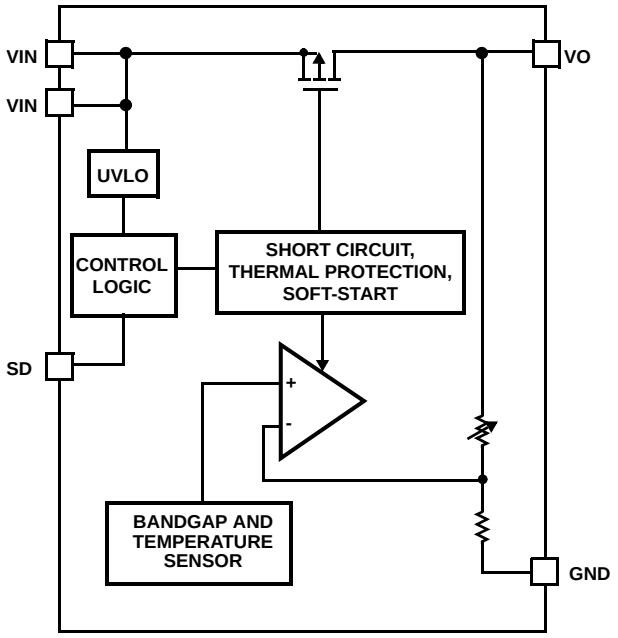
PIN NUMBER	PIN NAME	DESCRIPTION
1	VO	LDO Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended)
2, 3, 4	NC	No Connection
5	GND	GND is the connection to system ground. Connect to PCB Ground plane.
6	SD	LDO Shutdown. When this signal goes high, the LDO is turned off.
7	VIN	Supply Voltage/LDO Input: Connect a 1µF capacitor to GND.
8	VIN	Supply Voltage/LDO Input: Connect a 1µF capacitor to GND.

Typical Application



C_1, C_2: 1µF X5R CERAMIC CAPACITOR

Block Diagram



Functional Description

The ISL9007 contains all circuitry required to implement a high performance LDO. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9007 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, and soft-start. Smart thermal shutdown protects the device against overheating. Soft-start minimize start-up input current surges without causing excessive device turn-on time.

Power Control

The ISL9007 has a shutdown pin (SD) to control power to the LDO output. When SD is high, the device is in shutdown mode. In this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1µA. When the SD pin goes low, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least 2.1V (typical). Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry turn-on. Once the references are stable, the LDO powers up.

During operation, whenever the VIN voltage drops below about 1.84V, the ISL9007 immediately disables both LDO outputs. When VIN rises back above 2.1V (assuming the SD pin is low), the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter.

The bandgap generates a zero temperature coefficient (TC) voltage for the regulator reference and other voltage references required for current generation and over-temperature detection.

A current generator provides references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9000 provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output

capacitor value above 4.7µF is not recommended as LDO performance improvement is minimal.

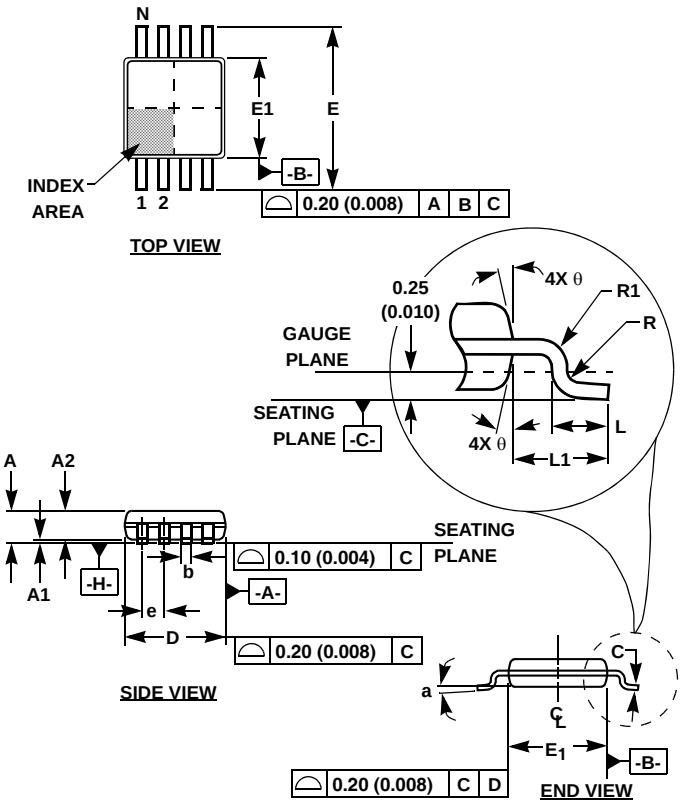
Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge. The ISL9007 provides short-circuit protection by limiting the output current to about 500mA.

The LDO uses an independently trimmed 1V reference as its input. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory to one of the following output voltages: 3.3, 2.85V, 2.8V, and 2.5V.

Overheat Detection

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +145°C, the LDO momentarily shuts down until the die cools sufficiently. In the overheat condition, if the LDO sources more than 50mA it will be shut off. Once the die temperature falls back below about +110°C, the disabled LDO is re-enabled and soft-start automatically takes place.

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.